IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Priority Application Serial No. 09/444,024
Priority Filing Date . . . . . November 19, 1999
Inventor . . . . . Jigish D. Trivedi et al.
Assignee . . . . . Micron Technology, Inc.
Priority Group Art Unit 2811
Priority Examiner . . . . . Douglas W. Owens
Attorney's Docket No. MI22-1965
Title: Integrated Circuitry

PRELIMINARY AMENDMENT

To: Box Patent Application
Assistant Commissioner for Patents
Washington, D.C. 20231

From: D. Brent Kenady (Tel. 509-624-4276; Fax 509-838-3424)
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AMENDMENTS

In the Specification

At p. 1 before the "Technical Field" section, please insert the following:

RELATED PATENT DATA

This application resulted from a continuation application of U.S. Patent Application Serial No. 09/444,024, filed November 19, 1999, entitled "P-Type FET in a CMOS With Nitrogen Atoms in the Gate Dielectric", naming Jigish D. Trivedi, Zhongze Wang and Rhongsheng Yang as inventors, which was a divisional application of Patent Application Serial No. 09/386,076, filed August 30, 1999, now Patent No. 6,093,661, issued July 25, 2000, entitled "Integrated Circuitry and

Semiconductor Processing Method of Forming Field Effect Transistors", naming Jigish D. Trivedi, Zhongze Wang and Rongsheng Yang as inventors, the disclosure of which is incorporated by reference.

In the Claims

Please cancel claims 1-37 and add claims 38-49 as follows:

CLAIMS

38. (New) Integrated circuitry comprising a semiconductor substrate having an area within which a plurality of n-type and p-type field effect transistors are formed, the respective transistors comprising a gate, a gate dielectric layer and source/drain regions, the gate dielectric layer of the p-type field effect transistors comprising an oxide having nitrogen atoms therein, and the nitrogen atoms being higher in concentration within the gate dielectric layer at only one elevational location as compared to another elevational location, the gate dielectric layer of the n-type field effect transistors being different in composition from the gate dielectric layer of the p-type field effect transistors.

39. (New) The integrated circuitry of claim 38 wherein the gate dielectric layer of the p-type transistors comprises silicon dioxide.

40. (New) The integrated circuitry of claim 38 wherein the gate dielectric layer of the p-type transistors are of a different thickness relative the gate dielectric layer of the n-type transistors.

41. (New) The integrated circuitry of claim 38 wherein the concentration of nitrogen atoms in the gate dielectric layer of the p-type transistors at the one elevational location is from 0.1% molar to 10.0% molar.

42. (New) The integrated circuitry of claim 38 wherein the one elevational location is located proximate an interface of the gate dielectric layer with the semiconductor substrate.

43. (New) Integrated circuitry comprising a semiconductor substrate having an area within which a plurality of n-type and p-type field effect transistors are formed, the respective transistors comprising a gate, a gate dielectric layer and source/drain regions, the gate dielectric layer of the p-type field effect transistors comprising silicon dioxide having nitrogen atoms therein, the nitrogen atoms being higher in concentration within the gate dielectric layer at only one elevational location as compared to another elevational location and at a concentration of from 0.1% molar to 10.0% molar, the gate dielectric layer of the n-type field effect transistors comprising silicon dioxide material proximate an interface of the gate dielectric layer with the semiconductor substrate which is substantially void of nitrogen atoms.

44. (New) The integrated circuitry of claim 43 wherein the one elevational location is located proximate an interface of the gate dielectric layer with the semiconductor substrate.

45. (New) Integrated circuitry comprising a semiconductor substrate substantially devoid of nitrogen atoms and having an area within which a plurality of n-type and p-type field effect transistors are formed, the respective transistors comprising a gate, a gate dielectric layer and source/drain regions, the gate dielectric layer of the p-type field effect transistors comprising an oxide having nitrogen atoms therein, the gate dielectric layer of the n-type field effect transistors being different in composition from the gate dielectric layer of the p-type field effect transistors.

46. (New) The integrated circuitry of claim 45 wherein the nitrogen atoms are higher in concentration within the gate dielectric layer at only one elevational location as compared to another elevational location.

47. (New) Integrated circuitry comprising a semiconductor substrate substantially devoid of nitrogen atoms and having an area within which a plurality of n-type and p-type field effect transistors are formed, the respective transistors comprising a gate, a gate dielectric layer and source/drain regions, the gate dielectric layer of the p-type field effect transistors comprising silicon dioxide having nitrogen atoms therein, the gate dielectric layer of the n-type field effect transistors comprising silicon dioxide material proximate an interface of the gate dielectric layer with the semiconductor substrate, the silicon dioxide material being substantially void of nitrogen atoms.

48. (New) The integrated circuitry of claim 47 wherein the nitrogen atoms being higher in concentration within the gate dielectric layer at only one elevational location as compared to another elevational location.

49. (New) The integrated circuitry of claim 47 wherein the nitrogen atoms being higher in concentration within the gate dielectric layer at only one elevational location as compared to another elevational location and at a concentration of from 0.1% molar to 10.0% molar.

REMARKS

Claims 1-37 have been canceled. Claims 38-49 have been added for consideration.

Claims 38-44 recite verbatim the language of claims 27-33, respectively, of the parent application. Such claims stand rejected under 35 U.S.C. §103(a) as being unpatentable over Soleimani et al. (U.S. Patent No. 5,596,218) in view of Gardner et al. (U.S. Patent No. 6,225,151). Applicant traverses such rejections.

Claim 38 recites a gate dielectric layer of n-type field effect transistors being different in composition from a gate dielectric layer of the p-type field effect transistors. The Examiner correctly states that Soleimani does not teach the gate dielectric of the n-type field effect transistor is different in composition from the gate dielectric of the p-type field effect transistor (Pg. 2 of Paper No. 15 of the parent application). The Examiner then relies on the combination of Gardner with Soleimani alleging that Gardner teaches that it is beneficial to provide nitrogen atoms as a boron diffusion barrier in p-**channel** transistors, and that Gardner further teaches that nitrogen atoms near the **channel** of n-channel IGFETs can have a detrimental affect on the performance of the transistor (Pg. 2 of Paper No. 15 of the parent application). From these alleged teachings, the Examiner concludes that it would have been obvious to one of ordinary skill in the art to avoid including nitrogen atoms in the area near the channel of the n-channel transistors since it is desirable to obtain optimal performance from the device (Pg. 2-3 of Paper No. 15 of the parent application). The Examiner relies on the phrase "to avoid including nitrogen atoms in the area near the channel

of the n-channel transistors" to allege such teaches avoiding nitrogen atoms in the gate dielectric layer of the n-channel transistors (Pg. 3 of Paper No. 15 of the parent application). The Examiner concludes that avoiding nitrogen atoms in the gate dielectric layer of the n-channel transistors teaches the above-stated limitation of claim 38. (Pg. 3 of Paper No. 15 of the parent application). Applicants disagree.

Respectfully, the Examiner is reminded that an appropriate prior art reference used for an obviousness rejection must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. MPEP §2141.02 citing to *W.L. Gore & Associates, Inc. vs. Garlock, Inc.*, 721 F.2d 1540, 220, USPQ 303 (Fed. Cir. 1983). The Examiner's entire argument relies on the inference that the phrase "to avoid including nitrogen atoms in the area near the channel" teaches avoiding nitrogen in a gate dielectric layer formed over the channel. However, the Gardner teaching for which the Examiner is relying is stated as:

> Limiting the nitrogen implant to the N-well 605 has other advantages. For example, the **drive current** of N-channel IGFETs may be negatively affected by significant concentration of nitrogen in and near the channel (emphasis added).

Column 11, lines 64-67. Importantly, Gardner is addressing how nitrogen affects the drive current of a transistor. One skilled in the art understands that the drive current occurs in the channel of a transistor, and the channel is formed in the semiconductor substrate beneath the gate dielectric layer (col. 11, lines 14-67). Consequently, no reasonable or fair interpretation of the teachings of Gardner could suggest that avoiding nitrogen atoms in the area near the channel

would include the gate dielectric layer where no drive current exists, and therefore, the Examiner's inference must fail. Considering Gardner in its entirety, i.e., as a whole, in no reasonable or fair interpretation could Gardner suggest or teach a gate dielectric layer of n-type field effect transistors being different in composition from a gate dielectric layer of the p-type field effect transistors as recited in claim 38. Given that it has already been established that Soleimani does not teach such limitation of claim 38, it is inconceivable that the combination of Soleimani and Gardner could teach such limitation of claim 38. Since the combination of art fails to teach a positively recited limitation of claim 38, the obviousness rejection fails and should be withdrawn. For at least this reason, claim 38 is allowable.

Moreover, the entire disclosure of Gardner teaches providing nitrogen regions or liners in the **channels or below the source/drain regiongs** of transistors (col. 3, lines 45-67; col. 7, lines 12-30; col. 7, lines 45-66; etc.; Figs. 1B-1E, Figs. 2B-2C; Figs. 3B, 3D; Figs. 4A-4B; etc), and is completely devoid of teachings to nitrogen provided in the gate dielectric layer as recited in claim 38. In fact, the only teaching to nitrogen relative the gate dielectric layer is an implanted nitrogen-rich region formed beneath the source/drain regions as well as below the gate dielectric region within the channel region 101 of semiconductor body 100 (col. 8, lines 5-15; Figs. 4A-4B). Consequently, considering Gardner in its entirety, i.e., as a whole, and in combination with Soleimani, in no reasonable or fair interpretation could Gardner suggest or teach a gate dielectric layer of n-type field effect transistors being different in composition from a gate dielectric layer of the p-type field effect transistors as

recited in claim 38. Even the title of Gardner supports such which is stated as: Nitrogen Liner beneath Transistor Source/Drain Regions to retard Dopant Diffusion. Since the combination of art fails to teach a positively recited limitation of claim 38, the obviousness rejection fails and should be withdrawn. For at least this reason, claim 38 is allowable.

Additionally, obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggesting, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. MPEP §2143.01 citing to *In re Fine,* 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *In re Jones,* 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). "Preferably the Examiner's explanation should be such that it provides that impetus necessary to cause one skilled in the art to combine the teachings of the references to make the proposed modification." *Ex Parte Levengood,* 28 USPQ2d, 1300, 1301, Footnote 2, (Bd. Pat. App. and Inter. 1993) (citations omitted).

The Examiner has presented a motivational rationale for the combination of Soleimani and Gardner as: it would have been obvious to one of ordinary skill in the art to avoid including nitrogen atoms in the area near the channel of the n-channel transistors since it is desirable to obtain optimal performance from the device formed on the wafer. However, Gardner teaches that the **drive current** of N-channel IGFETs may be negatively affected by significant concentration of nitrogen in and near the channel (emphasis added) (col. 11, lines 64-67). As argued previously, the drive current does not exist in the gate

dielectric layer, only in the channel of the transistor formed in the substrate. Consequently, Gardner (and thus the combination with Soleimani) does not teach or suggest any performance characteristic regarding nitrogen in the gate dielectric layer, whether beneficial or detrimental. Therefore, the motivational rationale presented by the Examiner to combine the art, that is, because it is desirable to obtain optimal performance from the device, does not exist. Since a proper obviousness rejection requires a proper motivational rationale for the combination, and the Examiner has not presented one, the obviousness rejection must fail. For at least this reason, claim 38 is allowable. Applicant respectfully requests allowance of claim 38 in the next Office Action.

Claims 39-42 depend from independent claim 38, and therefore, are allowable for the reasons discussed above with respect to the independent claim, as well as for their own recited features which are neither shown or taught by the art of record.

Claim 43 recites a gate dielectric layer of n-type field effect transistors comprising silicon dioxide material proximate an interface of the gate dielectric layer with the semiconductor substrate which is substantially void of nitrogen atoms. Soleimani teaches a CMOS device that includes PMOS and NMOS transistors and the gate oxides for each type of transistor having a region of nitrogen atoms (col. 4, lines 36-49; Figs. 5-6). Gardner teaches providing nitrogen liners or regions below source/drain regions of transistor devices. In no fair interpretation could Soleimani or Gardner, singularly or in any combination, teach or suggest a gate dielectric layer of n-type field effect transistors comprising silicon dioxide material proximate an interface of the gate dielectric

layer with the semiconductor substrate which is substantially void of nitrogen atoms as recited in claim 43. Consequently, the combination of Soleimani and Gardner fail to teach a positively recited limitation of claim 43, and therefore, claim 43 is allowable. Applicant respectfully requests allowance of claim 43 in the next Office Action.

Moreover, the Examiner has presented a motivational rationale for the combination of Soleimani and Gardner as: it would have been obvious to one of ordinary skill in the art to avoid including nitrogen atoms in the area near the channel of the n-channel transistors since it is desirable to obtain optimal performance from the device formed on the wafer. However, Gardner teaches that the **drive current** of N-channel IGFETs may be negatively affected by significant concentration of nitrogen in and near the channel (emphasis added) (col. 11, lines 64-67). As argued previously, the drive current does not exist in the gate dielectric layer, only in the channel of the transistor formed in the substrate. Consequently, Gardner (and thus the combination with Soleimani) does not teach or suggest any performance characteristic regarding nitrogen in the gate dielectric layer, whether beneficial or detrimental. Therefore, the motivational rationale presented by the Examiner to combine the art, that is, because it is desirable to obtain optimal performance from the device, does not exist. Since a proper obviousness rejection requires a proper motivational rationale for the combination, and the Examiner has not presented one, the obviousness rejection must fail. For at least this reason, claim 43 is allowable. Applicant respectfully requests allowance of claim 43 in the next Office Action.

Claim 44 depends from independent claim 43, and therefore, is allowable for the reasons discussed above with respect to the independent claim, as well as for its own recited features which are neither shown or taught by the art of record.

This application is now believed to be in immediate condition for allowance, and action to that end is respectfully requested. If the Examiner's next anticipated action is to be anything other than a Notice of Allowance, the undersigned respectfully requests a telephone interview prior to issuance of any such subsequent action.

Respectfully submitted,

Dated: 2-27-02

By: _____
D. Brent Kenady
Reg. No. 40,045

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Priority Filing Date ..... November 19, 1999
Inventor ..... Jigish G. Trivedi et al.
Assignee ..... Micron Technology, Inc.
Priority Group Art Unit 2811
Priority Examiner ..... Douglas W. Owens
Attorney's Docket No. MI22-1965
Title: Integrated Circuitry

VERSION WITH MARKINGS TO SHOW CHANGES MADE ACCOMPANYING PRELIMINARY AMENDMENT

In the Specification

The replacement specification paragraphs incorporate the following amendments. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

At p. 1 before the "Technical Field" section, please insert the following:

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This application resulted from a continuation application of U.S. Patent Application Serial No. 09/444,024, filed November 19, 1999, entitled "P-Type FET in a CMOS With Nitrogen Atoms in the Gate Dielectric", naming Jigish D. Trivedi, Zhongze Wang and Rhongsheng Yang as inventors, which was a divisional application of Patent Application Serial No. 09/386,076, filed August 30, 1999, now Patent No. 6,093,661, issued July 25, 2000, entitled "Integrated Circuitry and Semiconductor Processing Method of Forming Field Effect Transistors", naming Jigish D. Trivedi, Zhongze Wang and Rongsheng Yang as inventors, the disclosure of which is incorporated by reference.

In the Claims

The claims have been amended as follows. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

Please cancel claims 1-37 and add claims 38-49. There are no other amendments.

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